

an interconnect pattern which is electrically isolated from said contact hole and
said interconnect and which exists between said N-channel transistor and said
P-channel transistor,

C1
wherein said interconnect pattern is formed in an uppermost interconnect layer of
said CMOS basic cell.

23. (Amended) The CMOS basic cell of Claim 22, wherein said interconnect
pattern extending either along a perpendicular direction or along a horizontal direction
relative to a boundary between said N-channel transistor and said P-channel transistor.

C2
26. (Amended) The CMOS basic cell of any one of Claims 22 to 25, wherein two
or more said CMOS basic cells are electrically connected by a higher interconnect
pattern located in a layer that is higher than said interconnect pattern.

27. (Amended) The CMOS basic cell according to Claim 26, wherein said higher
interconnect pattern is located in a region between said P-channel transistors and said
N-channel transistors except the both ends of said interconnect pattern, and
wherein said interconnect pattern which intersects said higher interconnect
pattern is electrically connected with said higher interconnect pattern, said interconnect